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WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

(a) a semiconductor substrate;

(b) an insulating film formed at a surface of said semiconductor substrate for defining device regions in each of which a semiconductor device is to be fabricated;

(c) a gate electrode formed on said semiconductor substrate;

(d) a sidewall covering said gate electrode therewith; and

(e) drain and source diffusion layers formed at a surface of said semiconductor substrate around said gate electrode,

said sidewall having a sidewall offset extending outwardly of said gate electrode along a surface of said semiconductor substrate in at least one of regions below which said drain and source diffusion layers are to be formed,

at least one of said drain and source diffusion layers extending towards said gate electrode beyond an edge of said sidewall offset.

2. The semiconductor device as set forth in claim 1, wherein said sidewall offset is formed along a surface of said semiconductor substrate in both regions below which said drain and source diffusion layers are to be formed.

3. The semiconductor device as set forth in claim 1, further comprising second diffusion layers formed below said drain and source diffusion layers and surrounding said drain and source diffusion layers.

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4. The semiconductor device as set forth in claim 3, wherein said second diffusion layers have a lower impurity-concentration than that of said drain and source diffusion layers.

5. The semiconductor device as set forth in claim 1, further comprising a

memory cell formed on said semiconductor substrate.

6. A semiconductor device comprising:

(a) a semiconductor substrate;

(b) an insulating film formed at a surface of said semiconductor substrate for defining device regions in each of which a semiconductor device is to be fabricated;

(c) a gate electrode formed on said semiconductor substrate;

(d) a sidewall covering said gate electrode therewith;

(e) drain and source diffusion layers formed at a surface of said semiconductor substrate around said gate electrode; and

(f) low-resistive wiring layers formed at surfaces of said drain and source diffusion layers, said low-resistive wiring layers being located outwardly beyond a peripheral edge of said sidewall offset,

said sidewall having a sidewall offset extending outwardly of said gate electrode along a surface of said semiconductor substrate in at least one of regions below which said drain and source diffusion layers are to be formed,

at least one of said drain and source diffusion layers extending towards said gate electrode beyond an edge of said sidewall offset.

7. The semiconductor device as set forth in claim 6, wherein said low-resistive wiring layers are composed of TiSi.

8. The semiconductor device as set forth in claim 6, wherein said sidewall offset is formed along a surface of said semiconductor substrate in both regions below which said drain and source diffusion layers are to be formed.

9. The semiconductor device as set forth in claim 6, further comprising second diffusion layers formed below said drain and source diffusion layers and surrounding said drain and source diffusion layers.

10. The semiconductor device as set forth in claim 9, wherein said second diffusion layers have a lower impurity-concentration than that of said drain and source diffusion layers.

11. The semiconductor device as set forth in claim 6, further comprising a memory cell formed on said semiconductor substrate.

12. A method of fabricating a semiconductor device, comprising the steps of:

(a) forming an insulating film at a surface of a semiconductor substrate to thereby define device regions in which a semiconductor device is to be formed;

(b) forming a first well having a first electrical conductivity and a second well having a second electrical conductivity in a first region in which a first transistor is to be fabricated, and further forming a first well having a first electrical conductivity and a second well having a second electrical conductivity in a second region in which a second transistor is to be fabricated;

(c) forming a gate electrode of said first transistor in said first region and a gate electrode of said second transistor in said second region;

(d) forming first drain and source diffusion layers of said first and second transistors in both said first and second regions;

(e) forming a sidewall around said gate electrode of said first transistor, said sidewall having a sidewall offset having an edge remoter from said gate electrode than an edge of said first drain and source diffusion layers on at least one of said first drain and source diffusion layers, and forming a sidewall around said gate electrode of said second transistor; and

(f) forming second drain and source diffusion layers of said first transistor in both said first and second regions.

13. The method as set forth in claim 12, further comprising the step of lowering a resistance of at least a portion of said second drain and source diffusion

layers of said first transistor.

14. The method as set forth in claim 13, wherein said portion is turned into silicide.

15. The method as set forth in claim 12, wherein said sidewall offset is formed in both said first drain and source diffusion layers in said step (e).

16. A method of fabricating a semiconductor device, comprising the steps of:

(a) forming an insulating film at a surface of a semiconductor substrate to thereby define device regions in which a semiconductor device is to be formed;

(b) forming a first well having a first electrical conductivity and a second well having a second electrical conductivity in a first region in which a first transistor is to be fabricated, forming a first well having a first electrical conductivity and a second well having a second electrical conductivity in a second region in which a second transistor is to be fabricated, and forming a well in a third region in which a memory cell is to be fabricated;

(c) forming a gate electrode of said memory cell in said third region;

(d) forming a diffusion layer of said memory cell in said third region;

(e) forming a gate electrode of said first transistor in said first region and a gate electrode of said second transistor in said second region;

(f) forming first drain and source diffusion layers of said first and second transistors in both said first and second regions;

(g) forming a sidewall around said gate electrode of said first transistor, said sidewall having a sidewall offset having an edge remoter from said gate electrode than an edge of said first drain and source diffusion layers on at least one of said first drain and source diffusion layers, and forming a sidewall around said gate electrode of said second transistor; and

(h) forming second drain and source diffusion layers of said first transistor in

both said first and second regions.

17. The method as set forth in claim 16, further comprising the step of lowering a resistance of at least a portion of said second drain and source diffusion layers of said first transistor.

18. The method as set forth in claim 17, wherein said portion is turned into silicide.

19. The method as set forth in claim 16, wherein said sidewall offset is formed in both said first drain and source diffusion layers in said step (g).

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